

WHAT IS CLAIMED IS:

1                   1.       An apparatus to provide a substantially linear relationship  
2 between an input signal and a selected parameter, the apparatus comprising:  
3                   a square root converter couplable to receive the input signal, the  
4 square root converter adapted to provide a square root signal, the square root signal  
5 substantially proportional to a square root of the input signal; and  
6                   a logarithmic generator couplable to receive the input signal and  
7 coupled to the square root converter, the logarithmic generator adapted to provide  
8 an applied signal, the applied signal substantially proportional to a sum of a  
9 logarithm of the input signal plus the square root signal.

1                   2.       The apparatus of claim 1, further comprising:  
2                   a voltage-to-current converter coupled to the square root converter  
3 and to the logarithmic generator, the voltage-to-current converter couplable to  
4 receive an input voltage and adapted to provide the input signal as an input current  
5 having a substantially linear relationship to the input voltage.

1                   3.       The apparatus of claim 2, wherein the voltage-to-current  
2 converter further comprises:  
3                   an operational amplifier having a first input coupled to receive the  
4 input voltage; and  
5                   a n-channel transistor coupled to an output and to a second input of  
6 the operational amplifier, the n-channel transistor adapted to provide the input  
7 current.

1                   4.       The apparatus of claim 1, wherein the logarithm of the input  
2 signal is provided by the logarithmic generator as substantially equivalent to a  $3/2$   
3 power of the input signal.

1                   5.       The apparatus of claim 1, further comprising:  
2                   a current mirror coupled to the voltage-to-current converter, to the  
3 square root converter and to the logarithmic generator, the current mirror adapted

4 to provide the input current from the voltage-to-current converter to the square root  
5 converter and the logarithmic generator.

1 6. The apparatus of claim 1, further comprising:  
2 an amplifier coupled to the logarithmic generator to provide an  
3 amplified applied signal.

1 7. The apparatus of claim 1, wherein the applied signal has a  
2 non-linear relationship to the selected parameter.

1 8. The apparatus of claim 1, wherein the input signal is an input  
2 voltage or an input current linearly converted from the input voltage.

1 9. The apparatus of claim 1, wherein the selected parameter is  
2 a frequency response.

1 10. The apparatus of claim 1, further comprising:  
2 a parallel plate capacitor coupled to receive the applied signal,  
3 wherein the selected parameter is a frequency response of the parallel plate  
4 capacitor, and wherein the frequency response varies substantially linearly with the  
5 applied signal.

1 11. The apparatus of claim 1, further comprising:  
2 a varactor coupled to receive the applied signal, wherein the selected  
3 parameter is a frequency response of the varactor, and wherein the frequency  
4 response varies substantially linearly with the applied signal.

1 12. The apparatus of claim 11, wherein the varactor is a CMOS-  
2 compatible MEMS varactor.

1 13. The apparatus of claim 1, wherein the selected parameter is  
2 a capacitance.

1                   14.    The apparatus of claim 1, wherein the square root converter  
2 is coupled through a buffer to the logarithmic generator.

1                   15.    The apparatus of claim 1, wherein the square root converter  
2 further comprises a first n-channel MOSFET transistor and a second n-channel  
3 MOSFET transistor having a nested-pair configuration and having coupled gates to  
4 receive the input signal.

1                   16.    The apparatus of claim 1, wherein the square root converter  
2 further comprises:  
3                   a first transistor having a first gate, a first drain and a first source;  
4                   a second transistor having a second gate, a second drain and a second  
5 source, the first gate coupled to the second gate to receive the input signal, the  
6 second drain coupled to the first source to provide the square root signal.

1                   17.    The apparatus of claim 1, wherein the logarithmic generator  
2 further comprises a transistor having a gate to receive the square root signal and  
3 having a source couplable to receive the input signal.

1                   18.    The apparatus of claim 17, wherein the transistor is a p-  
2 channel transistor adapted to operate in a weak inversion state.

1                   19.    The apparatus of claim 1, wherein the applied signal is a  
2 voltage level  $V_p$ , wherein the voltage level  $V_p = c\sqrt{V_{DC}} + d \ln\left(\frac{V_{DC}}{e}\right)$ , wherein  $V_{DC}$  is an  
3 input voltage level provided as the input signal, and wherein  $c$ ,  $d$ , and  $e$  are  
4 predetermined constants.

1                   20.    The apparatus of claim 1, further comprising:  
2                   an oscillator coupled to receive the applied signal, wherein an  
3 oscillation frequency of the oscillator is the selected parameter and is substantially  
4 linearly tunable in response to the applied signal.

1                   21.     A circuit to provide a substantially linear relationship between  
2     an input voltage and a frequency response of a capacitor, the circuit comprising:  
3                   a voltage-to-current converter, the voltage-to-current converter  
4     couplable to receive the input voltage, the voltage-to-current converter capable of  
5     providing an input current substantially linearly proportional to the input voltage;  
6                   a current mirror coupled to the voltage-to-current converter; and  
7                   a square root converter coupled to the current mirror to receive the  
8     input current, the square root converter capable of providing a first output voltage  
9     substantially proportional to a square root of a magnitude of the input current.

1                   22.     The circuit of claim 21, further comprising:  
2                   a junction varactor coupled to receive the first output voltage,  
3     wherein a capacitance of the junction varactor varies substantially linearly with the  
4     input voltage to provide a linear frequency response.

1                   23.     The circuit of claim 1, further comprising:  
2                   a logarithmic generator coupled to the square root converter to  
3     receive the first output voltage and coupled to the current mirror to receive the input  
4     current, the logarithmic generator capable of providing a second output voltage  
5     substantially proportional to a superposition of a logarithm of the magnitude of the  
6     input current with the square root of the magnitude of the input current.

1                   24.     The circuit of claim 23, further comprising:  
2                   a parallel plate capacitor coupled to receive the second output voltage,  
3     wherein a frequency response of the parallel plate capacitor varies substantially  
4     linearly with the input voltage.

1                   25.     The circuit of claim 23, further comprising:  
2                   a CMOS-compatible varactor coupled to receive the second output  
3     voltage, wherein a frequency response of the CMOS-compatible varactor varies  
4     substantially linearly with the input voltage.

1                   26.    An apparatus to provide a substantially linear relationship  
2 between an input voltage and a predetermined circuit parameter, the apparatus  
3 comprising:

4                   a voltage-to-current converter, the voltage-to-current converter  
5 couplable to receive the input voltage, the voltage-to-current converter capable of  
6 providing an input current substantially linearly proportional to the input voltage;

7                   a current mirror coupled to the voltage-to-current converter;

8                   a square root converter coupled to the current mirror to receive the  
9 input current, the square root converter capable of providing a first output voltage  
10 substantially proportional to a square root of a magnitude of the input current;

11                  a logarithmic generator coupled to the current mirror to receive the  
12 input current, the logarithmic generator capable of providing a second output  
13 voltage substantially proportional to a logarithm of the magnitude of the input  
14 current; and

15                  a combiner coupled to the square root converter to receive the first  
16 output voltage and coupled to the logarithmic generator to receive the second output  
17 voltage, the combiner adapted to provide an applied signal substantially equal to a  
18 sum of the logarithm of the magnitude of the input current plus the square root of  
19 the magnitude of the input current, wherein the applied signal has a substantially  
20 nonlinear relationship to the predetermined parameter.

1                   27.    A method of providing a substantially linear relationship  
2 between an input voltage and a predetermined circuit parameter, the method  
3 comprising:

4                   converting the input voltage to an input current, wherein the input  
5 current is substantially linearly proportional to the input voltage;

6                   generating a square root voltage from the input current, wherein the  
7 square root voltage is substantially proportional to a square root of a magnitude of  
8 the input current;

9                   generating a logarithmic voltage from the input current, wherein the  
10 logarithmic voltage is substantially proportional to a logarithm of the magnitude of  
11 the input current, and wherein the logarithmic voltage is substantially equal to a  $3/2$   
12 power of the input current; and

13 combining the square root voltage and the logarithmic voltage to form  
14 an applied signal substantially equal to a sum of the square root voltage and the  
15 logarithmic voltage, wherein the applied signal has a substantially nonlinear  
16 relationship to the predetermined parameter; and  
17 applying the applied signal to vary the predetermined circuit  
18 parameter substantially linearly with the input voltage.

1 28. A method to create a substantially linear relationship between  
2 an input signal and a selected parameter, comprising:  
3 (a) receiving the input signal;  
4 (b) determining a square root of a magnitude of the input signal  
5 to form a square root signal;  
6 (c) determining a logarithm of the magnitude of the input signal  
7 to form a logarithmic signal;  
8 (d) combining the square root signal with the logarithmic signal  
9 to form an applied signal; and  
10 (e) providing the applied signal for adjustment of the selected  
11 parameter substantially linearly with the input signal.

1 29. The method of claim 28, wherein the logarithm of the  
2 magnitude of the input signal is provided as a substantial approximation to a  $3/2$   
3 power of the magnitude of the input signal.

1 30. A method to create a substantially linear relationship between  
2 an input signal and a selected parameter, comprising:  
3 (a) receiving the input signal;  
4 (b) determining a square root of a magnitude of the input signal  
5 to form a square root signal;  
6 (c) determining a  $3/2$  power of the magnitude of the input signal  
7 to form a power signal;  
8 (d) combining the square root signal with the power signal to  
9 form an applied signal; and

10 (e) providing the applied signal for adjustment of the selected  
11 parameter substantially linearly with the input signal.

1 31. An apparatus comprising:  
2 an interface to convert an analog input signal to a digital input signal  
3 and to convert a digital applied signal to an analog applied signal, wherein the  
4 interface is further adapted to provide the analog applied signal for adjustment of a  
5 selected parameter substantially linearly with the analog input signal; and  
6 a processor coupled to the interface, the processor adapted to  
7 determine a square root of a magnitude of the digital input signal to form a square  
8 root signal; to determine a logarithm of the magnitude of the input signal to form  
9 a logarithmic signal; and the processor further adapted to combine the square root  
10 signal with the logarithmic signal to form the digital applied signal.

1 32. A processor adapted to process a tuning signal to form a  
2 processed signal and to provide the processed signal to control a displacement of a  
3 plate of a micromachined varactor as a substantially linear function of the tuning  
4 signal.

1 33. The processor of claim 32 wherein the processor is further  
2 adapted to process the tuning signal by determining a square root of a magnitude of  
3 the input signal to form a square root signal, determining a logarithm of the  
4 magnitude of the input signal to form a logarithmic signal, and combining the square  
5 root signal with the logarithmic signal to form the processed signal.

1 34. The processor of claim 32 wherein the processor is further  
2 adapted to process the tuning signal by determining a square root of a magnitude of  
3 the input signal to form a square root signal, determining a  $3/2$  power of the  
4 magnitude of the input signal to form a power signal, and combining the square root  
5 signal with the power signal to form the processed signal.

1                   35.    A method of controlling a displacement of a plate of a  
2 micromachined varactor, the method comprising:  
3                   processing the tuning signal to form a processed signal; and  
4                   providing the processed signal to control the displacement wherein  
5 the tuning signal is processed so that displacement of the plate is a substantially  
6 linear function of the tuning signal.

1                   36.    The method of claim 35, wherein the processing of the tuning  
2 signal further comprises determining a square root of a magnitude of the input signal  
3 to form a square root signal, determining a logarithm of the magnitude of the input  
4 signal to form a logarithmic signal, and combining the square root signal with the  
5 logarithmic signal to form the processed signal.

1                   37.    The method of claim 35, wherein the processing of the tuning  
2 signal further comprises determining a square root of a magnitude of the input signal  
3 to form a square root signal, determining a  $3/2$  power of the magnitude of the input  
4 signal to form a power signal, and combining the square root signal with the power  
5 signal to form the processed signal.